Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) A method for testing interconnections of a circuit having at least one DC coupled interconnection and at least one AC coupled ~~interconnects~~ interconnection, ~~of a~~ the circuit having at least one driving IC and at least one receiving IC that are capacitively coupled together by at least one AC coupled interconnection, each IC having a plurality of boundary scan cells (BSCs), an instruction register, and a TAP controller, the method comprising the steps of:

evaluating a test type signal and effecting an AC interconnection test if the test type signal is set, the AC interconnection test comprising:

shifting an AC test stimulus into the BSCs of the at least one driving IC, the AC test stimulus having a plurality of voltage transitions;

scanning an initiate AC test instruction into the instruction register of both ICs;

performing an execute AC test instruction by moving the TAP controller to the *Run-Test/Idle* state and holding the TAP controller of both ICs in the *Run-Test/Idle* state for the time required to complete execution of the AC test instruction, wherein, during the *Run-Test/Idle* controller state, the at least one driving IC is applying the AC test stimulus to the at least one AC coupled interconnection and the at least one receiving IC is sampling a received signal embodying captured AC test instruction results;

transferring the captured AC test instruction results into the BSCs of the at least one receiving IC;

scanning out the captured AC test instruction results if the Test type signal is set; and;

effecting a DC interconnection test if the test type signal is not set.

2. (Currently amended) The method as defined in claim 1, wherein the AC interconnection test further ~~comprising~~ comprises the step of evaluating the captured AC test instruction results.

3. (Currently amended) The method as defined in claim 1, wherein the AC interconnection test further ~~comprising~~ comprises the step of generating a second AC test stimulus and repeating the steps of shifting, scanning, performing, transferring and scanning out with the second AC test stimulus.

4. (Currently amended) The method as defined in claim 3, , wherein the AC interconnection test further ~~comprising~~ comprises the step of evaluating the captured AC test instruction results for the second AC test stimulus.

5. (Currently amended) A system for testing interconnections of a circuit having at least one DC coupled interconnection and at least one AC coupled ~~interconnects~~ interconnection, ~~of a~~ the circuit having at least one driving IC and at least one receiving IC that are capacitively coupled together by at least one AC coupled interconnection, each IC having a plurality of boundary scan cells (BSCs), an instruction register, and a TAP controller, the system comprising:

means for evaluating a test type signal, initiating an AC interconnection test if the test type signal is set and initiating a DC interconnection test if the test type signal is not set;

means for shifting an AC test stimulus into the BSCs of the at least one driving IC, the AC test stimulus having a plurality of voltage transitions;

means for scanning an initiate AC test instruction into the instruction register of both ICs;

means for performing an execute AC test instruction by moving the TAP controller to the *Run-Test/Idle* state and holding the TAP controller of both ICs in the *Run-Test/Idle* state for the time required to complete execution of the AC test instruction, wherein, during the *Run-Test/Idle* controller state, the at least one driving IC is applying the AC test stimulus to the at least one AC coupled interconnection and the at least one receiving IC is sampling a received signal embodying captured AC test instruction results;

means for transferring the captured AC test instruction results into the BSCs of the at least one receiving IC; ~~and~~

means for scanning out the captured AC test instruction results; and

means for effecting a DC interconnection test.

6. (Original) The system as defined in claim 5, further comprising means for evaluating the captured AC test instruction results.

7. (Original) The system as defined in claim 5, further comprising means for generating a second AC test stimulus.

8. (Original) The system as defined in claim 7, further comprising means for evaluating the captured AC test instruction results for the second AC test stimulus.

9-12. (Canceled)

13. (Currently amended) A system for testing interconnections of a circuit having at least one DC coupled interconnection and at least one AC coupled ~~interconnects~~ interconnection comprising:

at least one driving IC having a plurality of boundary scan cells (BSCs), an instruction register, and a TAP controller;

at least one receiving IC having a plurality of BSCs, an instruction register, and a TAP controller; ~~and~~

at least one AC coupled interconnection that capacitively couples the at least one driving IC to the at least one receiving IC;

at least one DC coupled interconnection; and

a test type signal generator configured to generate a test type signal;

wherein the BSCs of the at least one driving IC are capable of receiving an AC test stimulus having a plurality of voltage transitions, the instruction register of both ICs are capable of receiving an initiate AC test instruction, the TAP controller of both ICs is capable of being moved to and held in the *Run-Test/Idle* state for the time required to complete execution of the AC test instruction, wherein, during the *Run-Test/Idle* controller state, the at least one driving IC is applying the AC test stimulus to the at least one AC coupled interconnection and the at least one receiving IC is sampling a received signal embodying captured AC test instruction results, and the BSCs of the at least one receiving IC are capable of receiving and scanning out the captured AC test instruction results if the test type signal is set, and wherein a DC interconnection test is effected if the signal is not set.

14-26. (Canceled)

27. (New) A method for testing interconnections of a circuit having at least one DC coupled interconnection and at least one AC coupled interconnection, comprising:

evaluating a test type signal;

effecting an AC interconnection test if the test type signal is set; and

effecting a DC interconnection test if the test type signal is not set.

28. (New) The method of claim 27 wherein the circuit includes at least one driving IC and at least one receiving IC that are capacitively coupled together by at least one AC coupled interconnection, each IC having a plurality of boundary scan cells (BSCs), an instruction register, and a TAP controller, and the AC interconnection test includes shifting an AC test stimulus into the BSCs of the at least one driving IC, the AC test stimulus having a plurality of voltage transitions, scanning an initiate AC test instruction into the instruction register of both ICs, performing an execute AC test instruction by moving the TAP controller to the *Run-Test/Idle* state and holding the TAP controller of both ICs in the *Run-Test/Idle* state for the time required to complete execution of the AC test instruction, wherein, during the *Run-Test/Idle* controller state, the at least one driving IC is applying the AC test stimulus to the at least one AC coupled interconnection and the at least one receiving IC is sampling a received signal embodying captured AC test instruction results, transferring the captured AC test instruction results into the BSCs of the at least one receiving IC, scanning out the captured AC test instruction results and evaluating the captured AC test instruction results.

29. (New) A system for testing interconnections of a circuit having at least one DC coupled interconnection and at least one AC coupled interconnection, comprising:

means for evaluating a test type signal;

means for effecting an AC interconnection test if the test type signal is set; and

means for effecting a DC interconnection test if the test type signal is not set.

30. (New) The system of claim 29 wherein the circuit includes at least one driving IC and at least one receiving IC that are capacitively coupled together by at least one AC coupled interconnection, each IC having a plurality of boundary scan cells (BSCs), an instruction register, and a TAP controller, and the AC interconnection test includes shifting an AC test stimulus into the BSCs of the at least one driving IC, the AC test stimulus having a plurality of voltage transitions, scanning an initiate AC test instruction into the instruction register of both ICs, performing an execute AC test instruction by moving the TAP controller to the *Run-Test/Idle* state and holding the TAP controller of both ICs in the *Run-Test/Idle* state for the time required to complete execution of the AC test instruction, wherein, during the *Run-Test/Idle* controller state, the at least one driving IC is applying the AC test stimulus to the at least one AC coupled interconnection and the at least one receiving IC is sampling a received signal embodying captured AC test instruction results, transferring the captured AC test instruction results into the BSCs of the at least one receiving IC, scanning out the captured AC test instruction results and evaluating the captured AC test instruction results.